wherein, in a planar layout of the ferroelectric memory device, the first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, and does not cover at least one side of the rectangular top electrode, and [the distance between the top electrode and another top electrode adjacent to the top electrode is smaller than the width of a bit line formed above the top electrode] the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode.

REMARKS

Claims 1-10 are pending in this application. By this Amendment, claim 1 is amended. Reconsideration in view of the above amendments and following remarks is respectfully solicited.

Entry of the amendments is proper under 37 CFR §1.116 since the amendments: (a) place the application in condition for allowance (for the reasons discussed herein); (b) do not raise new issues requiring further search and/or consideration (since the amendments amplify issues previously discussed throughout prosecution); (c) satisfy a requirement of form asserted in the previous Office Action; (d) do not present any additional claims without canceling a corresponding number of finally rejected claims; and/or (e) place the application in better form for appeal, should an appeal be necessary. Entry of the amendments is thus respectfully requested.

I. THE CLAIMS SATISFY THE REQUIREMENTS OF 35 U.S.C. §112, 1st PARAGRAPH

The Office Action rejects claims 1-10 under 35 U.S.C. §112, first paragraph. This rejection is respectfully traversed.

Applicants respectfully submit that the amendment to claim 1 obviates the rejection under 35 U.S.C. §112, first paragraph. In particular, in order to correct a clerical error, claim 1 is amended to recite, *inter alia,* the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode. For example, Figure 1 shows that the width of a bit line formed above the top

electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode.

The Office Action alleges that the phrase "the top electrode having a rectangular planar pattern" is not described in the specification and the Figures. In other words, the Office Action seems to assert that the planar pattern of the top electrode is not rectangular. However, Applicants respectfully submit that the term "rectangular" means a flat shape with four straight sides forming four right angles, including a square. As such, Applicants' disclosure does indeed describe the claimed top electrode having a rectangular planar pattern, as set forth in claim 1.

Accordingly, withdrawal of the rejection of claims 1-20 under 35 U.S.C. §112, first paragraph is respectfully solicited.

II. THE CLAIMS DEFINE PATENTABLE SUBJECT MATTER

The Office Action rejects claims 1-10 under 35 U.S.C. §103(a) as unpatentable over Applicant's Prior Art (hereinafter APA) in view of U.S. Patent No. 5,869,859 to Hanagasaki. This rejection is respectfully traversed.

Applicants respectfully submit that APA, either alone or in combination with Hanagasaki, fails to teach or suggest each and every feature as set forth in the claimed invention. In particular, both APA and Hanagasaki fail to teach or suggest the width of a bit line formed above the top electrode is smaller than the distance between the top electrode and another top electrode adjacent to the top electrode, as set forth in amended claim 1.

Independent claim 1 is amended to recite, *inter alia,* a nonvolatile semiconductor memory device with a ferroelectric capacitor in which first interconnection layer partially overlaps with the top electrode of the ferroelectric capacitor, not covering at least one side of the rectangular top electrode, so as to eliminate deterioration in characteristics of the ferroelectric capacitor.

The APA teaches a nonvolatile semiconductor memory device with a ferroelectric capacitor in which a first interconnection layer forming a storage line overlaps with the top electrode of the ferroelectric capacitor, and covers two opposite sides of the rectangular top electrode. The APA further teaches that, in a planar layout, a bit line crosses at right angle with two opposite sides of the rectangular top electrode and overlaps with the top electrode, covering the two opposite sides of the top electrode.

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The presently claimed invention, as recited in claims 1-10, is distinguishable from the APA because the present invention teaches a first interconnection layer that overlaps with a top electrode and does not cover at least one side of the rectangular top electrode of the capacitor, while the APA teaches that the storage line and the bit line overlap with the top electrode of the capacitor and covers all the four sides of the rectangular top electrode.

The Office Action attempts to use Hanagasaki in order to solve the deficiencies of the APA. However, Hanagasaki discloses a DRAM memory cell with a dielectric capacitor in which the capacitor is formed on a field oxide film, and a silicon nitride film having a high dielectric constant is used as a capacitor dielectric layer. A gate insulating film of a transistor and part of a capacitor dielectric layer of the capacitor are formed at the same time, and the gate electrode of the transistor and an upper capacitor electrode of the capacitor are formed at the same time. Applicants respectfully submit that the object of Hanagasaki is to lessen the process load and to reduce the cell size of a memory.

However, the presently claimed invention is distinguished over Hanagasaki for the following reasons. First, as shown in Figure 1, Hanagasaki discloses a structure in which an interconnection 11 connecting a drain region 9b of the transistor and an upper electrode 8b of the capacitor overlaps with the upper electrode 8b, covering one side of the upper electrode 8b. Next, as is clear from Figure 3, Hanagasaki fails to disclose interconnections between upper electrodes to the capacitor, between C1 and C2 adjacent to each other, and between C2 and C3 adjacent to each other. On the other hand, the presently claimed invention, as illustrated in Figures 1 and 2, discloses not only that a storage line 20 connecting to a doped layer 13 of the memory cell transistor and to a top electrode 18, partially overlaping the top electrode 18 covering part of the top electrode 18, but also that the width of a bit line DB connected to the doped layer 13 of the memory cell is smaller than the distance between the top electrode 18 and another adjacent top electrode.

Thus, Applicants submit that Hanagasaki fails to teach the arrangement of the bit line of the presently claimed invention. Even if Hanagasaki is combined with the APA, it is impossible to achieve the device of the present invention. Applicants submit that if Hanagasaki is applied to the APA, it is possible to obtain the structure in which the storage line 60 connecting source/drain doped layers 53 and the a top electrode 58 overlaps with the top electrode 58, covering one side of the top electrode 58. However, because Hanagasaki fails to disclose any

line above the upper electrode, it is impossible to obtain that the distance between two electrodes of the ferroelectric capacitor which are adjacent to each other is larger than the width of the bit line formed above the upper electrode, as now recited in independent claim 1. Accordingly, Applicants submit that claims 1-10, as amended, are not obvious over Hanagasaki, even in combination with the APA.

Applicants respectfully submit that independent claim 1 is patentable over APA in view of Hanagasaki. Since claims 2-10 depend on amended claim 1, claims 2-10 are also patentable over the cited references. Accordingly, withdrawal of the rejection of claims 1-10 under 35 U.S.C. §103(a) is respectfully solicited.

III. CONCLUSION

In view of the foregoing, Applicants respectfully submit that the application is in condition for allowance. Favorable reconsideration and prompt allowance are earnestly solicited.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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